

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	762	(712/23).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:22
S2	486	(712/215).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:22
S3	0	(superscalar\$1) same (issu\$3 with way\$1 with group\$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:23
S4	7	(issu\$3 with way\$1 with (instruction\$1 near4 group\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:26
S5	0	(issu\$3 with (instruction\$1 near4 group\$3)) same (mutiple\$1 near4 (process\$3 or function\$3) near4 (unit\$1 or device\$1 or element\$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:27
S6	0	(issu\$3 with instruction\$1 with (simultaneous\$2 or concurrent\$2)) same (mutiple\$1 near4 (process\$3 or function\$3) near4 (unit\$1 or device\$1 or element\$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:27
S7	0	(issu\$3 with instruction\$1 with (simultaneous\$2 or concurrent\$2)) same (mutiple\$1 near4 (process\$3 or function\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:28
S8	0	(issu\$3 with instruction\$1 with (simultaneous\$2 or concurrent\$2)) same (mutiple\$1 with (process\$3 or function\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:28
S9	1	(issu\$3 with instruction\$1 with (simultaneous\$2 or concurrent\$2)) and (mutiple\$1 with (process\$3 or function\$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:28
S10	132	(issu\$3 with instruction\$1 with (simultaneous\$2 or concurrent\$2)) and (integer near4 (float\$3?point\$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:29
S11	16	(issu\$3 with instruction\$1 with (simultaneous\$2 or concurrent\$2)) same (integer near4 (float\$3?point\$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:39

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S12	8	(("6038656") or ("5752070") or ("6044061") or ("5832303") or ("6230228") or ("5802055") or ("6279065") or ("6301630")).PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:32
S13	775	(712/23).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:33
S14	516	(712/215).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:34
S15	728	(712/23).CCLS.	US-PGPUB; USPAT	OR	OFF	2007/03/25 10:34
S16	520	(712/215).CCLS.	US-PGPUB; USPAT	OR	OFF	2007/03/25 10:34
S17	1	("20040111589").PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:36
S18	0	(asynchronous\$5) near4 (issu\$3 near4 instruction\$1 near4 simultaneous\$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:38
S19	0	(asynchronous\$5) with (issu\$3 near4 instruction\$1 near4 simultaneous\$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:39
S20	0	(asynchronous\$5) with (issu\$3 with instruction\$1 with simultaneous\$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:39
S21	0	(asynchronous\$5) same (issu\$3 with instruction\$1 with simultaneous\$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:39
S22	0	(asynchronous\$5 near4 pipeline\$3) and (issu\$3 with instruction\$1 with simultaneous\$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 11:57
S23	37	(issu\$3 with instruction\$1 with (simultaneous\$2 or concurrent\$2)) same (integer near4 (float\$3?point\$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:40

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S24	14	(issu\$3 with instruction\$1 with (simultaneous\$2 or concurrent\$2)) same (integer near4 (float\$3?point\$1)) and ((asynchronous or independent) near4 pipelin\$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:40
S25	2	((lines-andrew\$) and (southworth-robert\$) and (cummings-uri\$)).in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:44
S26	63	((lines-andrew\$) or (southworth-robert\$) or (cummings-uri\$)).in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:44
S27	5	(asynchronous\$5 near4 pipelin\$3) same (sequential\$4 near4 control\$5)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 11:57

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... algorithm on both synchronous and **asynchronous** (self-timed ... and Fisher [2] verifies a **pipeline** circuit with ... Constraints Next, we consider the **Issue** of fairness. ...
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... To solve this problem, we have added an additional **pipeline** register
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... level, where clock distribution is not an **Issue**. Interboard communications have long used **asynchronous** links (for ... processing delay among all **pipeline** stages. ...
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... a lookup on every instruction address **Issue** it is ... nism stalls a **control** loop in the **execution pipeline**. ... and RAM are self-timed for **asynchronous** operation using ...
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